Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A flip chip package substrate, comprising:
a plurality of patterned circuit layers, wherein two outmost layers of the patterned circuit layers form a plurality of first contacts on a first surface of the flip chip package substrate and form a plurality of second contacts on a second surface of the flip chip package substrate, and wherein the first contacts are electrically connected to the second contacts;
a plurality of dielectric layers, each dielectric layer being disposed between any two adjacent patterned circuit layers, wherein the patterned circuit layers and the dielectric layers are arranged alternatively; and
a plurality of bumps, disposed on the first surface of the flip chip package substrate, wherein each bump is connected to one corresponding first contact, and wherein the bumps are to be connected to a chip.

[c2] 2. The substrate of claim 1, further comprising a plurality of solder balls disposed on the second surface of the flip chip package substrate, wherein the solder balls connect to the second contacts.

[c3] 3. The substrate of claim 1, further comprising a plural-

ity of pins disposed on the second surface of the flip chip package substrate, wherein the pins connect to the second contacts.

[c4] 4. The substrate of claim 1, wherein two solder mask layers are respectively arranged on the first and second surfaces of the flip chip package substrate, while the first and second contacts are exposed by the two solder mask layers.

[c5] 5. The substrate of claim 1, wherein a material of the bumps includes tin/lead alloy.

[c6] 6. A flip chip package process, comprising:
providing a substrate having a first surface and an opposite second surface, wherein the substrate includes a plurality of first contacts on the first surface of the substrate and a plurality of second contacts on the second surface of the substrate, and wherein the first contacts are electrically connected to the second contacts;
forming a plurality of bumps on the first surface of the substrate, wherein each bump is connected to one first contact;
providing a chip having a plurality of bonding pads corresponding to the bumps, wherein a metal layer is disposed on surfaces of the bonding pads;
arranging the chip onto the first surface of the substrate

by flipping the chip, so that the bonding pads are connected to the bumps; and
reflowing the bumps.

[c7] 7. The process of claim 6, further comprising disposing a plurality of solder balls on the second surface of the substrate, wherein the solder balls are connected to the second contacts.

[c8] 8. The process of claim 6, further comprising disposing a plurality of pins on the second surface of the substrate, wherein the pins are connected to the second contacts.

[c9] 9. The process of claim 6, wherein the method for forming the bumps comprises implanting tin globes and treating surfaces of the first contacts with a flux before implanting the tin globes.

[c10] 10. The process of claim 6, wherein the method for forming the bumps comprises printing a tin paste onto surfaces of the first contacts and reflowing the tin paste..

[c11] 11. The process of claim 6, wherein the method for forming the bumps comprises forming the bumps on surfaces of the first contacts by electroplating, thus forming the bumps on the substrate without reflowing.

[c12] 12. The process of claim 6, wherein an adhesive layer is

formed on the surfaces of the bonding pads of the chip before the chip is arranged to the substrate, and wherein after the chip is arranged to the substrate, the adhesive layer wraps around the bumps.

[c13] 13. The process of claim 6, further comprising filling an underfill material between the chip and the substrate, wherein the underfill material covers the bumps.

[c14] 14. The process of claim 6, wherein the metal layer is a nickel layer formed by electroless plating.